REMARKS

In the Office Action dated January 7, 2005, the Examiner rejected claims 1, 2, 4, 10, and 11 under 35 U.S.C. § 102(b) and rejected claims 3, 5-9, and 13-18 under 35 U.S.C. § 103(a). Applicants respectfully traverse the claim rejections and request reconsideration.

A. Substance of Examiner Interview

On February 23, 2005, an Examiner Interview was conducted telephonically. Participants of the interview included Examiner Zarneke, and Applicants' representatives Lisa Schoedel and Jori Schiffman. No exhibits were shown nor demonstrations conducted. The participants discussed claim 1 and the references cited in the previous Office Action. Further, the participants discussed the amendment that has been made to claim 1. Applicants claim a slotted file including a plurality of platelets each having a semiconductor chip placed into a chip carrier, and epoxy sealing the plurality of platelets into the slotted file to form a permanent integrated circuit package. The cited references teach a housing having slots in which printed circuit boards (PCBs) can be inserted and removed.

As a result of the interview, an agreement was reached that an amendment to claim 1 indicating that epoxy is used to seal the platelets into the slotted file to form an integrated circuit package would overcome the art of record. Accordingly, claim 1 has been amended to clarify that the integrated circuit package is sealed with epoxy to form a single, enclosed integrated circuit package. No new matter has been added. Applicants submit that claims 1-11 and 13-18 are currently in condition for allowance. Therefore, Applicants request that the Examiner enter this amendment and issue a Notice of Allowance.

B. Response to the 35 U.S.C. § 102(b) Rejections

Claims 1, 2, 4, 10, and 11 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 3,614,541 ("Farrand"), U.S. Patent No. 3,631,325 ("Wenz"), U.S. Patent No. 4,214,292 ("Johnson"), and U.S. Patent No. 5,276,590 ("Budman"). In amended claim 1, Applicants recite a system for three-dimensional packaging of platelets. The system includes a slotted file and a plurality of platelets that fit into the slotted file. Each of the platelets includes a semiconductor chip placed into a chip carrier so that the semiconductor chip contacts a plurality of electrodes located in the chip carrier. The platelets are stacked in the slotted file and sealed with epoxy to form a three-dimensional integrated circuit package. As a result, a three-dimensional integrated circuit package may be formed that provides a very tight spacing tolerance between platelets and that minimizes damage to the platelets during the stacking process.

In contrast, Farrand, Wenz, Johnson, and Budman each describe a housing having slots in which PCBs can be inserted and removed. For instance, Farrand discloses that it is easy to replace a defective PCB with another PCB (column 3, lines 54-56). Wenz discloses that a PCB can be readily inserted into and removed from the housing without undue wear (column 1, lines 51-53). Johnson discloses a guide spring that facilitates insertion and removal of a PCB from a housing (columns 1, line 57 to column 2, line 7). Budman discloses a flexible PCB that can fit as a replacement for a rigid PCB (abstract). The flexible PCB may eliminate space restrictions imposed when modifying existing PCB designs (column 1, lines 38-41).

A PCB is a thin board to which electronic components are fixed by solder. (See, www.dictionary.com.) The electronic components may be semiconductor chips or any other

electronic components. For example, the three-dimensional integrated circuit package claimed by Applicants may be mounted on a PCB as described by Farrand, Wenz, Johnson, and Budman. PCBs are designed to be removed from the housing so that repairs and design changes can be made to the PCB without damaging the system in which the PCB is installed. Therefore, the PCBs are not sealed into the housing to form an integrated circuit package.

Since Farrand, Wenz, Johnson, and Budman all intend to allow for the removal of the PCBs from the housing, it would not be obvious to one of ordinary skill in the art to use an epoxy to seal the PCBs into the housing. Thus, the prior art does not anticipate or render obvious the presently claimed application. In fact, Farrand, Wenz, Johnson, and Budman each *teach away* from this feature. Because Farrand, Wenz, Johnson, and Budman do not show or suggest using an epoxy to seal the platelets into the slotted file to form a three-dimensional integrated circuit package, Farrand, Wenz, Johnson, and Budman do not show or suggest each and every element of claim 1. Accordingly, Applicants submit that Farrand, Wenz, Johnson, and Budman do not anticipate claim 1.

Claims 2, 4, 10, and 11 depend from claim 1. Accordingly, Applicants also submit that Farrand, Wenz, Johnson, and Budman do not anticipate claims 2, 4, 10, and 11 for at least the reasons set forth above.

In light of the above, Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 102(b).

C. Response to the 35 U.S.C. § 103(a) Rejections

Claims 3 and 5-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Farrand, Wenz, Johnson, and Budman in view of U.S. Patent No. 6,457,515 ("Vafai"). Claims

3 and 5-9 depend from claim 1.

As described above, Farrand, Wenz, Johnson, and Budman do not show or suggest sealing the platelets into the slotted file with epoxy to form a three-dimensional integrated circuit package. Vafai is cited for teaching the use of silicon as a heat sink material. (See, Office Action, page 5.) This teaching in Vafai fails to overcome the deficiencies in Farrand, Wenz, Johnson, and Budman. Accordingly, Applicants submit that claims 3 and 5-9 are not obvious in light of the combination of Farrand, Wenz, Johnson, and Budman and Vafai for at least the reasons set forth above.

Claims 13-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Farrand, Wenz, Johnson, and Budman in view of U.S. Patent No. 5,140,405 ("King"). Claims 13-18 depend from claim 1. King is cited for teaching a semiconductor assembly comprising a chip carrier having a floor and a frame that extends beyond the edges of the frame to form flanges. (See, Office Action, page 6.) Further, King is cited for the teaching that the flanges fit into grooves of a motherboard or other application. These teachings in King, however, fail to overcome the deficiencies in Farrand, Wenz, Johnson, and Budman. Accordingly, Applicants submit that claims 13-18 are not obvious in light of the combination of Farrand, Wenz, Johnson, Budman, and King for at least the reasons set forth above.

In light of the above, Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 103(a).

CONCLUSION

In light of the above amendments and remarks, Applicants submit that the present application is in condition for allowance and respectfully request notice to this effect. The Examiner is requested to contact Applicants' representative below if any questions arise or she may be of assistance to the Examiner.

Respectfully submitted,

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